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An Optimal Gated Integrator Circuitrybased On Dummy Switch,For High-Resolution Energy Spectroscopy.

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Abstract:*Modern experiments in the physical sciences use electronics to monitor, digitize and store analog signals. We will consider the analog front-end of ion beam detector whose job is to solve the ballistic deficit problem by integrating the signal until all the charge is collected from the detector. Such a circuit is called Gated Integrator. The key element that actually stores the analog signal is a capacitor. The stored signal is damaged by noise due to charge injection, clock feedthrough and leackage current. Several works have been done to prevent these noises. In this paper, to ensure nonlinearity of the Gated integrator less than 0.03%, a novel circuit based on two switch transistors, to cancel the leakage current in the reset switch, is added with a dummy switch,which allows toreduce the charge injection up to 0.6mV.*

Keywords*:Energy spectroscopy; Gated integrator; Charge injection; MOS Switch; Leakage current; Noise, dummy switch.*

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I. Introduction

Various type of detectors such as germanium detectors, silicon charged particle detectors, Si (Li) detectors, proportional counters, and scintillation detectors, are used to measure the energy and photon count of X-ray fluorescent photons. In the aim to improve the readout circuit of the detectors which consist of low output signal, current integration to accumulate signal in the purpose of improving signal-to-noise ratio, dynamic range and sensitivity, high-resolution energy spectroscopy systems were developed in many experiments. Many structures were proposed for the gated integrator with a bank of semi-Gaussian shaping amplifiers, for different detectors to acquire energy information in those systems. Compared with peak detecting ADCs in traditional energy spectroscopy systems for pulse amplitude analysis, a Gated integrator amplifier automatically eliminates the ballistic deficit effect caused by changes in charge collection time of the detectors[1, 3]. A beam current monitor (BCM) was needed to calibrate these detectors. Beams applied for treatment are weak, sometime less than 1pA.This of significance in the energy resolution and dead time at the short shaping time constants required for ultra-high counting rates. A gated integrator is typically used in a pulsed laser measurement. The device can provide shot-by-shot data, whichis often recorded by a computer via an A/D converter. The gated integrator is recommended in situations where the signal has a very low duty cycle, low pulse repetition rate, and high instantaneous count rates. The noise bandwidth of the gated integrator depends on the gate width: short gates will have wide bandwidths, and so will be noisy. This would suggest that longer gates would be preferred; however, the signal of interest may be very short-lived, and using a gate, which is much wider than the signal, will not improve the S/N.The gated integrator also behaves as a filter: the output of the gated integrator is proportional to the average of the input signal during the gate, so frequency components of the input signal, which have an integral number of cycles during the gate, will average to zero. Fast shaping operation of the GI involves charge injection, clock feed through and leakage current that creates noises on the output voltage of the GI. This effect can be negligible when studied high output voltage mode of the detectors. However, while studied the weak signal from the detectors, these noises should be cancel. Several works have been done to prevent these noises. One of the recent works consist in the usage of the transmission gates (TG) circuit, T-switch configuration etc. [2], [4]. This technic oparates very well for low change clock and for clock input voltage greather than certain value. But, while using a fast change clock to turn off the switch, the output voltage is too noisy and the TG technic is limited to achieve high-resolution energy spectroscopy. We propose in this paper a simple circuit to cancel charge injection, clock feed through and leakage current in the GI for fast clock change and for weak input voltage. The circuit consists of a dummy switch driven by the opposite signal clock (gate logic or trigger). The description of this technique will be done such as analytical equations and simulation results.

II. Gated Integrator for High-Resolution Energy Spectroscopy

The Block diagramFig.1 showsthe Model 673 Spectroscopy Amplifier system. Preamplifiers and semi-Gaussian shaping amplifiers amplify the detector signals. The output from the shaping amplifier is connectedinto a fast shaper to generate a trigger, which allows building the gate logic of the Gated integrator. The semi-Gaussian output at the same time is integrated on the feedback capacitor C_f. Then the peak value output of Gated integrator is acquired by a PXI based DAQ system.

The moment the Gaussian shaped pulse arrives, switch S_G is open first while switch $S_R$is closed, bringing the gated integrator output to be at ground level. Immediately, the Gaussian shaped pulse arrives, a trigger signal is generated. Switch S_G closes and S_R opens, and the semi-Gaussian signal is integrated on capacitor $C_f$as described in Eq. (1).

$$U_{GI} = \frac{1}{R_G C_f}\int_0^T U_{GA}(t)\,dt + \delta_0 \tag{1}$$

Where, U_{GA} and U_{GI} are the output of the Gaussian shaping amplifier and a Gated integrator, respectively. The integration period is set to last as long as the longest semi-Gaussian pulse duration. After the integration, switch S_G is off, and the output of the GI is held. Meanwhile, a busy signal is generated to avoid new triggers during the event processing, which is to minimize the spectral distortion caused by two or more ions arriving at the detector within one amplifier pulse width. The reset and busy signal are held until a shot-duration clear signal arrives, which is generated at the end of the acquisition process. For this real time system, the counting rates can be up to 100 kHz. It was reportedthat ballistic deficit affected systems with HPGeClover detectors and large area scintillators, which vary significantly in their charge collection[5, 6]. In this paper, for detectors having little ballistic deficit effects, like silicon strip detectors, the linear relationship between the Gaussian pulse height and the GI output is analyzed and caring for good linearity.

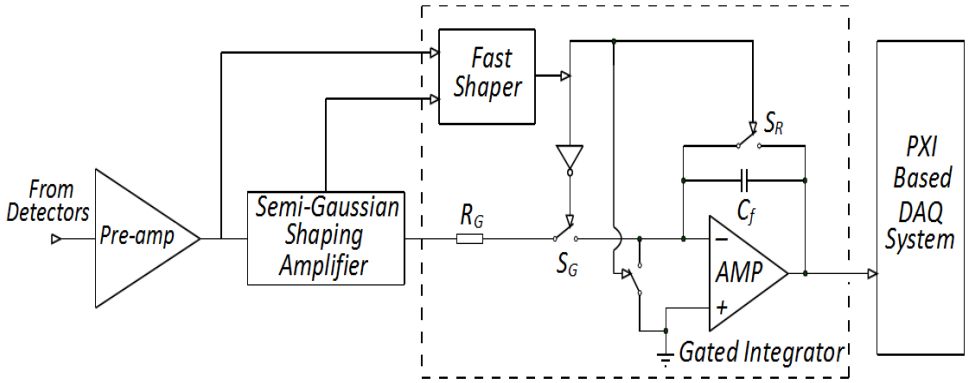

Fig1: Simplified Block Diagram of the Model 673 Spectroscopy Amplifier and Gated Integrator

III. The design of the new Gated integrator

A gated integrator is designed to receive the signal until all the charge is collected from the detector, and then recover fast, weak or strong analog signals with time scales ranging from *10ps to 100μs.* In a real application, a time window within a certain width is pulse gated after a set delay from an internal or external trigger. A gated integrator amplifies and integrates the signal that is present during the time the gate is open, excluding noise and interference that may be present at other times. Since any signal present while the gate is open will add linearly, while noise will add in a random manner as the square root of the number of shots, prevent leakage and charge injection compensation will improve the *SNR.*

3.1 Switch structure to avoid leakage current

The switch MOS is constructed and used to pass voltage or current. An ideal switch has the characteristics of zero resistance when it is on, infinite resistance when it is off and no delay when it is turned on or off. A real MOS switch however, has turn-on non-zero channel resistance, turn-off leakage current, parasitic capacitances and threshold voltage.

When the system is functioning and gated integrator is in recovering state, the effect reset switch has to be kept off. However, the effect of leakage current in the GI reset switch will induce errors to the output in the long duration of these states. The problem can be resolved by using the MOS switch configuration previously used to substitute single reset switch [4]. In this switch configuration, V_{DS} of the switch attached to the inverting input of the integrator is maintained at virtual *0 V*, and very little leakage current passes through this switch circuit, given by:

$$I_{DS} = KI_{DO} \cdot \exp\left(\frac{V_{GS} - V_{th}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (2)$$

$$I_{DO} = \mu_n C_{OX} (\eta - 1) V_T^2$$

Where $I_{DS}$is the drain to source current of the transistor MOS, K is the aspect ratio of the transistor, $I_{DO}$is the saturation current, $V_{GS}$is the gate to source voltage, $V_{th}$is the threshold voltage of a MOSFET, $V_T$is the thermal voltage, $V_{DS}$is the drain to source voltage, $\mu_n$is the carrier mobility, $C_{OX}$is the gate oxide capacitance, and η is the sub-threshold slope factor[8, 9]. Eq.(2) shows that, even for $V_{GS}=0$, the true way to obtain a zero switch leakage current is to set $V_{DS}$to *0 V*.

3-2 Charge injection cancellation circuit

The main characteristics of a MOS switch transistor are charge injection, clock feedthrough and switch speed. The rise and fall times of a submicron gate switch is usually less than *0.1 ns*. This causes a problem only in readout circuit of extremely high speed FPAs (Focal Plane Array). The charge injection and clock feedthrough however, are the main sources of noises in a MOS switch. How comes the charge injection and how to cancel it?

Instead of using, a transmission gate composed of a NMOS and a PMOS connected in parallel controlled by complementary signals, as a switch to replace each MOS in switch configuration [4]. Since it is known that the signs of the charges in an n-channel and in a p-channel are opposite, the charges injected from the n-channel and the p-channel cancel out each other if their areas of gates are carefully designed. To avoid this equity-designed task of areas of gates and reduce a number of component, we choose the option of a dummy switch configuration.

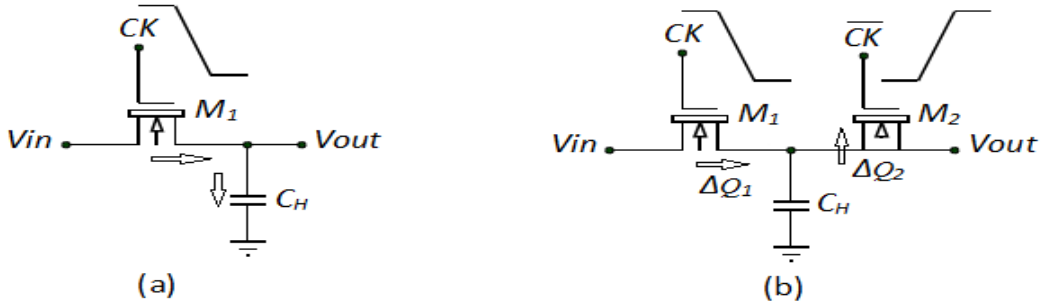

Fig.2: (a) Charge injection when a switch turns off, (b) Principe of cancelling charge injection

Let look at the Fig.2, to cancel the charge injected in Fig.2a, we have to calculate first the total charge injected in the channel of M_1, which is given by:

$$Q_{ch} = W_1 L_1 C_{OX} \left(V_{CK} - V_{in} - V_{TH1}\right) \quad (3)$$

This charge $Q_{ch}$is deposited on C_H and introduces an error in the voltage storage in the capacitor. The resulting error is then given by:

$$\Delta V = \frac{W_1 L_1 C_{OX}}{C_H}\left(V_{CK} - V_{in} - V_{TH1}\right) \quad (4)$$

To develop a new technique, we postulate that the charge injected by the main transistor can be removed while using a second transistor, called "dummy switch". As shown in Fig. 2b, dummy switch M_2, driven by opposite clock of the main transistor $M_1$is added to the circuit such that after M_1 turns off and M_2 turns on, the channel charge deposited by the transistor M_1 on $C_H$is absorbed by the latter M_2 to create a channel. Note that both the source and drain of $M_2$are connected to the output node [10].

In the process of the new designed gated integrator, Q_1 and Q_2 are respectively the charge injected by M_1 and M_2. We have the expressions:

$$Q_1 = W_1 L_1 C_{OX}\left(V_{CK} - V_{in} - V_{TH1}\right), \quad Q_2 = -2W_2 L_2 C_{OX}\left(V_{CK} - V_{in} - V_{TH2}\right) \quad (5)$$

The total charge injected in the channel by the two transistors is:

$Q_{total} = Q_1 + Q_2$. To cancel this, we should consider $Q_{total} = 0$ i.e. $W_1 L_1 = 2W_2 L_2$.

In CMOS technology process we have $L_1 = L_2$. So, $W_1 = 2W_2$

The circuit we propose for charge injection cancellation is shown in Fig.3.

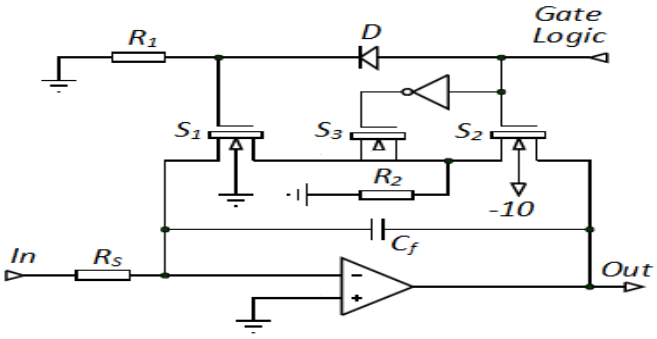

Fig. 3A optimal structure for Gated integrator

The basic method built on a switch transistor and a dummy switch, Fig.2b, can be apply here for optimal gated integrator, which is consisted of two switch transistors and one dummy switch so that, the charge injected by the channels of M_1, M_2 and M_3 should be zero, if we consider $W_1 + W_2 = 2W_3$.

Consequently, with the choice of $W_1 = W_2 = W_3$ and $L_1 = L_2$, the effect of clock feedthrough is suppressed. As presented in Fig. 3, considering the gate logic $V_{CK,}$ the total charge error in *Vout* is zero because,

$$V_{CK}\frac{W_1C_{OX}}{W_1C_{OX}+C_f+2W_2C_{OX}+W_3C_{OX}}-V_{CK}\frac{2W_3C_{OX}}{W_1C_{OX}+C_f+2W_2C_{OX}+W_3C_{OX}}+V_{CK}\frac{W_2C_{OX}}{W_1C_{OX}+C_f+2W_2C_{OX}+W_3C_{OX}}=0 \quad (6)$$

IV. Results and discussions

In order to recover the entire signal from the measurement system, Fig. 4, shows how a single switch does not prevent leakage current circle in the figureindicated by the dotted line. When, we substitute a single reset switch by MOS switch structure of two switch transistors, the simulation result in Fig. 5 shows the leakage current disappearance, but we still see an error appearance indicated by the dotted line circle in the figure. In the transition from *0* to $V_{in}+V_{th}$, the switch is off. Consequently, this part of the clock waveform can couple to $C_f$viaC_{GS}. As a result, a portion of the clock signal appears across $C_f$as indicated on the Fig. 5, during the transition. This problem is resolved by using a dummy switch placed carefully between the two switch transistors and result of simulation is presented in Fig. 6. Furthermore, the dummy switch can solve also, in contrary to charge injection when the switch is turned from on to off, there is charge absorption when the switch is turned from off to on, which causes an error too.

The measurements were developed in the laboratory in order to characterize DC and AC performances and efficiency of the circuit, which is built around Operational Amplifier AD713K-AD with good input noise current. The streaming signal generator XLV1 associated with voltage controlled current source was selected to supply the input current signal to GI on the software program PSPICE. Specification of the New GI is shown in table. Parameters were measured when the source current was in DC mode. All DC test results presented here and Fig.6 shows the waveform of the GI made by two switch transistors and a dummy switch. The linearity of the GI is shown in Fig.7.

Table
Specifications of the new GI.

Parameter	*Value*
Full scale output	*±5V*
Voltage conversion gain	*-1.0 V/V*
Linearity error	*<0.03%*
Output voltage noise	*<0.6mV (rms)*
Output offset voltage	*< 0.5mV (rms)*
Injected charge	*<50.4pc*
Temperature range	*-40 °C to 125°C*

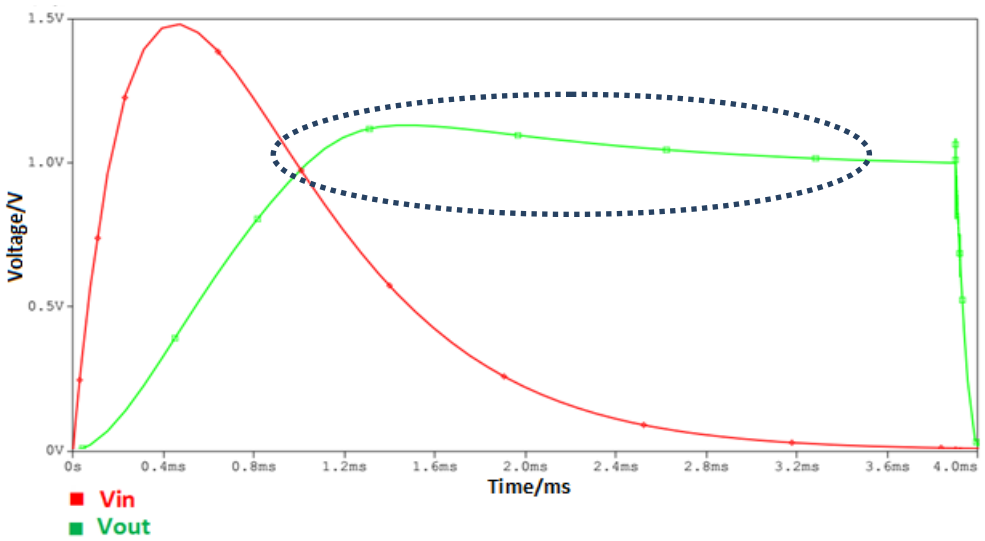

Fig. 4. Output waveform of the GI using a single reset switch

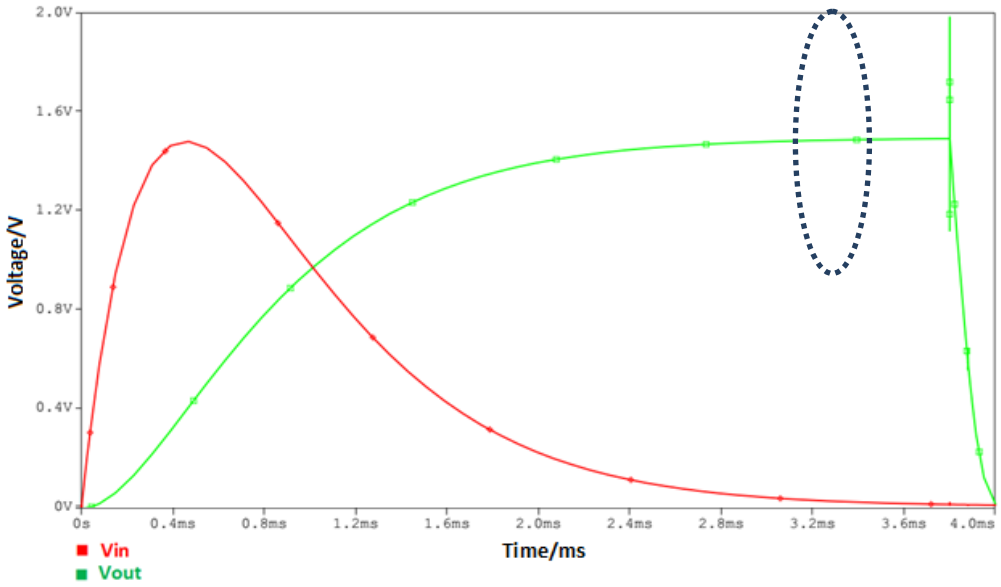

Fig. 5. Output waveform of the GI using switch structure made by two switch transistors [4]

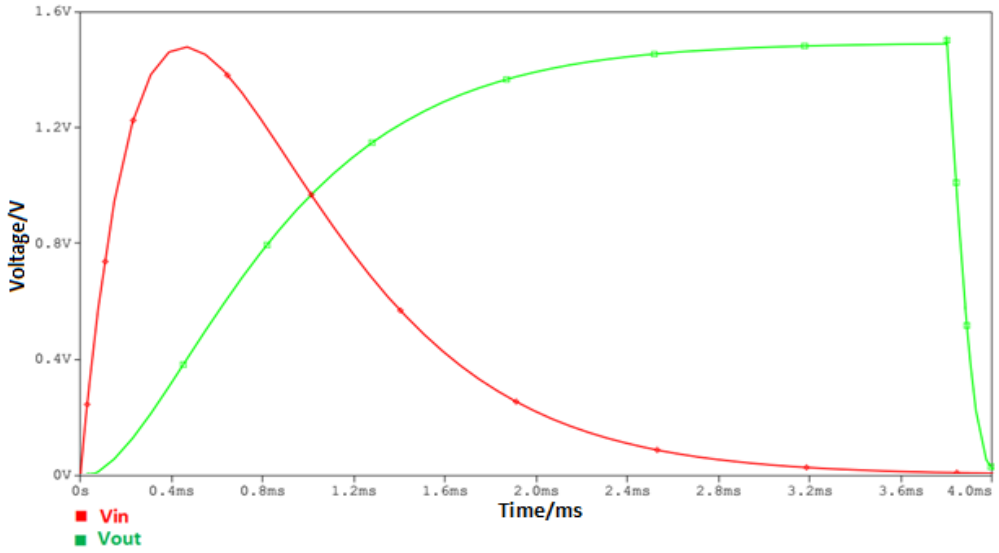

Fig 6. Output waveform of the GI using switch structure made by two-switch transistor and a dummy switch

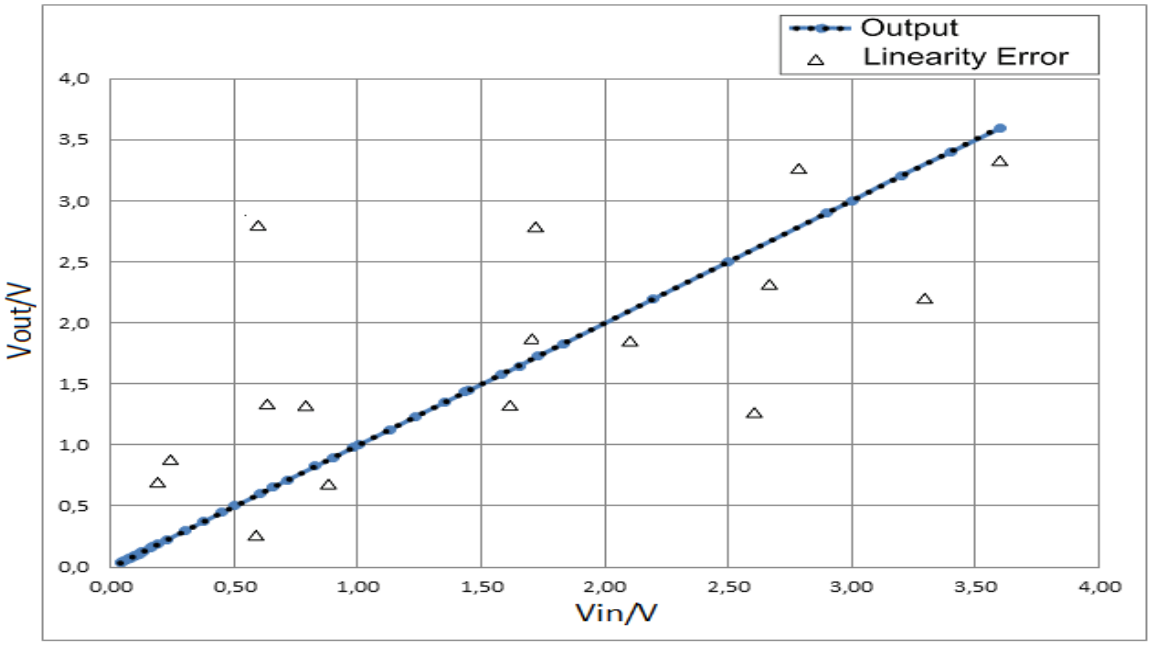

Fig. 7. Measured non-linearity of the GI.

V. Conclusions

With the new designed circuit, National instruments simulator carried out computer simulation. The high degree of linearity was achieved by using MOS switch structure, used as a new technique to prevent leakage current and at the same time reduce the charge injection from switches in the GI to *0.6mV*. The results of the simulation show how noise effect appears when we are measuring low values and disappear witha new circuit based on dummy switch. Because of the newcircuit, the simulation results insured that circuit would perform well in high-resolution energy spectroscopy systems.

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Author'sContributions

WembeTafoEvariste: Project leader, data interpretation and contribute to the writing of the paper.

FollaKamdemJérôme: Design and simulations model, data interpretationand contribute to the writing of the paper.

DjametYimga Arnaud: Design and simulations model. Also, contribute to the writing of the paper.

EssimbiZobo Bernard: Project leader. Revise and improve the final drafts of the paper.

Ethics

The corresponding author confirms that all of the other authors have read and approved the manuscript and no ethical issues involved.

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